Amendment to the Specification

Please replace Paragraphs [0047] to [0050] at page 2 with the following rewritten paragraphs:

-- **[0047]** Fig. 15 is a diagram ~~of a DLL~~ showing a bias circuit including a positive bias circuit and a negative bias circuit in accordance with an embodiment of the present invention;

[0048] Fig. 16 is a diagram ~~of bias circuits and delay~~ showing the negative bias circuit of Fig. 15;

[0049] Fig. 17 ~~illustrates the current bleeder device of Fig. 16~~ is a diagram showing the positive bias circuit of Fig. 15 and a delay cell; [[and]]

[0050] Fig. 18 ~~illustrates~~ is a diagram showing an implementation of the circuit of Figs. 16 and 17 [[.]];

[0050.1] Fig. 19 is a diagram showing the gate structure of a transistor included in the bias circuit of Fig. 17;

[0050.2] Fig. 20 is a diagram showing a delay lock loop (DLL) with the bias circuit of Fig. 17;

[0050.3] Fig. 21 is a diagram showing a phase lock loop (PLL) with the bias circuit of Fig. 17;

[0050.4] Fig. 22 is a diagram showing a charge pump with the bias circuit of Fig. 17;

[0050.5] Figs. 23a and 23b are diagrams showing an Operational Amplifier with the bias circuit of Fig. 17; and

[0050.6] Fig. 24 is a diagram showing an Input/Output pad with the bias circuit of Fig. 17. --

Please add the following paragraph after Paragraph [0080] at page 16:

-- **[0080.1]** Fig. 19 illustrates the gate structure of the transistor 528 of Fig. 17. As described above, the gate structure of the transistors 528 includes a plurality of stripes. In Fig. 19, stripes 802_1-802_N are shown as examples. Fig. 20 illustrates a basic DLL 804 with the bias circuit 600 of Fig. 17. Referring to Fig. 20, the DLL 804 includes a phase/frequency detector 806, a loop filter 808 and a VCDL 810. The bias circuit 600 of Fig. 17 is provided to the VCDL 810. Fig. 21 illustrates a basic PLL 820 with the bias circuit 600 of Fig. 17. Referring to Fig. 21, the PLL 820 includes a phase/frequency detector 826, a charge pump circuit 828, a loop filter 830 and a Voltage Controlled Oscillator (VCO) 832 using a VCDL. The bias circuit 600 of Fig. 17 is provided to the VCO 832. Fig. 22 illustrates a charge pump with the bias circuit 600 of Fig. 17. Referring to Fig. 22, the charge pump 840 includes the bias circuit 600 of Fig. 17, a charge pump stage 842 and a loop filter 844. Figs. 23a and 23b illustrate a basic Operational Amplifier 850 with the bias circuit 600 of Fig. 17. Fig. 24 illustrates an Input/Output pad 860 with the bias circuit 600 of Fig. 17. Referring to Fig. 24, the Input/Output pad module 860 includes an input receiver 862 and an output receiver 864. In Fig. 24, the bias circuit 600 of Fig. 17 is connected to the input receiver 862. --